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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/820,189	04/06/2004	Kyu Hyun Choi	021801-001110US	7411

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EXAMINER	
LEE, CALVIN	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 08/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/820,189	CHOI, KYU HYUN	
	Examiner	Art Unit	
	Lee Calvin	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *4/6/04* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

OFFICE ACTION

Drawings

1. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawing is required in reply to the Action.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b). Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer.

3. Claims 1-11 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-11 of copending Application No. 10/819,596. Although the conflicting claims are not identical, they are not patentably distinct from each other because the conflicting claim 1, with its first 12 process steps including the step of "forming lightly doped areas in the body region," clearly anticipates the examined claim 1 and its

process steps including the 10th step of "delivering first implants to the body region to form lightly doped areas in the body region."

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

4. Claim 1 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of US Patent 6,806,148 to *Choi et al* in view of US Patent 5,668,034 to *Sery et al.* Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 1 of *Choi et al* '148, with its process steps, reads on the examined claim 1 and its process steps such as:

-forming at least two isolation regions in the semiconductor substrate **100**;

-forming a well **114** between the two isolation regions to define a body region;

-forming a first oxide layer **118** above a first portion of the body region;

-forming a first dielectric layer **120**, **122** above the first oxide layer;

-forming above the first dielectric layer a first polysilicon layer **124** to form a control gate of a non-volatile device;

-forming a second dielectric layer **126** above the first polysilicon layer;

-forming a first spacer **132** above the body region and adjacent the first polysilicon layer;

-forming a second oxide layer **134**, **136**, **138** above a second portion of the body region not covered by the first spacer;

-forming a second polysilicon layer **144** over the second oxide layer, the first spacer **132**, and a portion of the second dielectric layer **126**; the second polysilicon layer forms a guiding gate **152a**, **152b** of the non-volatile device and a gate **148**, **150**, **154**, **156** of a MOS transistor;

-forming a second spacer **172** above the body region to define regions receiving lightly dopes implants and to define a conducting region of a capacitor of the non-volatile cell [¶ 0055].

-delivering second implants to the defined source and drain regions **174**, **176**, **178**, **180**.

However, claim 1 of *Choi* '148 lacks the step of "delivering first implants to the body region to form lightly doped areas in the body region." Nevertheless, such lightly doped areas are known in the semiconductor processing art as evidenced by *Sery et al* disclosing to form LDD **25** [Fig. 3D] and **57** [Fig. 5C] before the formation of source/drain regions **26** and **58** for the purpose of forming a barrier-rectifying junction with the S/D regions of the device.

Claim Rejections - 35 U.S.C. § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the U.S. only if the international application designated the U.S. and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-11 are rejected under 35 U.S.C. 102(**e**) as being anticipated by *Choi* (US 2005/0136592).

a) *Choi* '592 discloses a method of making an integrated circuit in a semiconductor substrate:

-forming at least two isolation regions [Fig. 8] in the semiconductor substrate **100**;

-forming a well **114** between the two isolation regions, the well defining a body region [Fig. 9];

-forming a first oxide layer **118** above a first portion of the body region [Fig. 11];

-forming a first dielectric layer **120**, **122** above the first oxide layer;

-forming above the first dielectric layer a first polysilicon layer **124** to form a control gate of a non-volatile device [Fig. 12];

-forming a second dielectric layer **126** above the first polysilicon layer;

-forming a first spacer **132** above the body region and adjacent the first polysilicon layer [Fig. 13];

-forming a second oxide layer **134**, **136**, **138** above a second portion of the body region not covered by the first spacer [Fig. 14];

-forming a second polysilicon layer **144** over the second oxide layer, the first spacer **132**, and a portion of the second dielectric layer **126**; the second polysilicon layer forms a guiding gate **152a**, **152b** of the non-volatile device and a gate **148**, **150**, **154**, **156** of a MOS transistor [Figs. 15-17];

-delivering first implants to the body region to form lightly doped areas **162**, **164**, **166**, **168**, **170** in the body region [Fig. 18];

-delivering second implants to the defined source and drain regions **174**, **176**, **178**, **180** [Fig. 19];

-forming a second spacer **172** above the body region to define regions receiving lightly dopes implants and to define a conducting region of a capacitor of the non-volatile cell [¶ 0055].

b) In re claim 2, *Choi* also discloses forming a salicide layer **182** over the portions of the lightly doped areas in the body region that form polysilicon landing pads [Fig. 20 and ¶ 0056].

c) In re claim 3, *Choi* also discloses forming a metal layer over the salicide layer to form a bit line **192** and a terminal adapted to receive a supply voltage [Fig. 22 and ¶ 0058].

d) In re claim 4, *Choi* also discloses a doping concentration of the first implants delivered to one of the source and drain regions of the non-volatile device is greater than a doping concentration of the first implants delivered to the other one of the source and drain regions of the non-volatile device [¶ 0054].

e) In re claim 5, *Choi* also discloses the first dielectric layer further includes an oxide layer **122** and a nitride layer **120** [¶ 0045].

f) In re claim 6, *Choi* also discloses the second dielectric layer **126** further includes an oxide and a nitride layer [¶ 0045 on page 4].

g) In re claims 7-10, *Choi* suggests an n-well formed below and before the p-well [¶ 0042]; wherein the n-well is formed using at least one implant step [¶ 0043] and/or at least two implant step using same mask [¶ 0044, last line].

h) In re claim 11, *Choi* also discloses the second oxide layer **136** has its thickness (120-250Å) greater than the thickness (15-40Å) of the first oxide layer **118**.

7. Claims 1-11 are rejected under 35 U.S.C. 102(e) as being anticipated by *Choi et al* (US 6,806,148).

a) *Choi et al* '148 discloses a method of making an integrated circuit in a substrate:

-forming at least two isolation regions [Fig. 8] in the semiconductor substrate **100**;

-forming a well **114** between the two isolation regions, the well defining a body region [Fig. 9];

-forming a first oxide layer **118** above a first portion of the body region [Fig. 11];

-forming a first dielectric layer **120**, **122** above the first oxide layer;

-forming above the first dielectric layer a first polysilicon layer **124** to form a control gate of a non-volatile device [Fig. 12];

-forming a second dielectric layer **126** above the first polysilicon layer;

-forming a first spacer **132** above the body region and adjacent the first polysilicon layer [Fig. 13];

-forming a second oxide layer **134**, **136**, **138** above a second portion of the body region not covered by the first spacer [Fig. 14];

-forming a second polysilicon layer **144** over the second oxide layer, the first spacer **132**, and a portion of the second dielectric layer **126**; the second polysilicon layer forms a guiding gate **152a**, **152b** of the non-volatile device and a gate **148**, **150**, **154**, **156** of a MOS transistor [Figs. 15-17];

-delivering first implants to the body region to form lightly doped areas **162**, **164**, **166**, **168**, **170** in the body region [Fig. 18];

-delivering second implants to the defined source and drain regions **174**, **176**, **178**, **180** [Fig. 19];

-forming a second spacer **172** above the body region to define regions receiving lightly dopes implants and to define a conducting region of a capacitor of the non-volatile cell [col. 9, ln.28].

b) In re claim 2, *Choi* also discloses forming a salicide layer **182** over the portions of the lightly doped areas in the body region that form polysilicon landing pads [Fig. 20 and col. 9].

c) In re claim 3, *Choi* also discloses forming a metal layer over the salicide layer to form a bit line **192** and a terminal adapted to receive a supply voltage [Fig. 22].

d) In re claim 4, *Choi* also discloses a doping concentration of the first implants delivered to one of the source and drain regions of the non-volatile device is greater than a doping concentration of the first implants delivered to the other one of the source and drain regions of the non-volatile device [col. 9, ln.20].

e) In re claim 5, *Choi* also discloses the first dielectric layer further includes an oxide layer **122** and a nitride layer **120** [col. 6, ln.55].

f) In re claim 6, *Choi* also discloses the second dielectric layer **126** further includes an oxide and a nitride layer [col. 6, ln.60].

g) In re claims 7-10, *Choi* suggests an n-well formed below and before the p-well [col.6, ln.9] wherein the n-well is formed using at least one implant step [col. 6, ln.30] and/or at least two implant step using same mask [col. 6, ln.43].

h) In re claim 11, *Choi* also discloses the second oxide layer **136** has its thickness (120-250Å) greater than the thickness (15-40Å) of the first oxide layer **118**.

Contact Information

8. Any inquiry concerning this communication from the Examiner should be directed to *Calvin Lee* at (571) 272-1896 on Mondays thru Thursdays 6:30-4:30 (EST). If attempts to reach the examiner by telephone are unsuccessful, Art Unit 2818's Supervisory Patent Examiner *David Nelms* can be reached at (571) 272-1787. The central fax number for the organization (where this application is assigned to) is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system at http:/pair-direct.uspto.gov. Should you have questions on access to the PAIR system, contact the Electronic Business Center at (866) 217-9197.

Calvin Lee

Dated: July 29, 2005